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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,910	12/30/2003	Kulwinder Dhanoa	15114H-071400US	1395

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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,910	DHANOA, KULWINDER	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, lines 1-2, the recitation of "wherein the or each bus" is unclear in the context of the claim. It appears that the recitation should be "wherein ~~the~~ said each bus".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson et al. (US Patent 6,279,064) in view of Schulz (US Patent 6,959,374).

As per claims 1, 7 and 13, Bronson teaches a memory controller system, method and programmable logical device, comprising:

an I/O bus unit, the I/O bus unit being for connection to an I/O device for receiving memory access requests (Figure 1 and column 3, line 26 to column 5, line 22, where "I/O bus unit" is read on "at least one bus interface" and "I/O device" is read on "at least one respective device");

a memory manager, for connection to a memory device over a memory bus (Figure 1 and column 5, lines 45-52, where "memory manager" is read on "memory interface");

two sets of data buffers (column 3, line 26 to column 5, line 22, where "two sets of data buffers" is read on " a plurality of buffers");

a control logic, for placing received memory access requests into a queue manager (Figure 1 and column 3, line 26 to column 5, line 44, where "queue manager" is read on "queue of memory access requests"); and

the memory manager perform real memory access honoring request for the I/O (column 5, lines 54-52).

Bronson does not teaches the memory controller system, method and programmable logical device, comprising:

a plurality of buffers, wherein in response to a received memory access request requiring multiple data bursts over the memory bus, data from each of said multiple data bursts is stored in a respective buffer of said plurality of buffers.

Schulz teaches a memory controller system, method and programmable logical device, comprising:

a cache memory (Figure 2, where "cache memory" is read on "plurality of buffers"); and

responding to a read request requiring multiple data burst over the memory bus, data from each of said multiple data bursts is stored in a respective memory of said cache memory (Figure 1 and column 1, line 65 to column 2, line 10, where "read quest" is read on "memory access request").

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Bronson to include for the memory controller system, method and programmable logical device, comprising:

a cache memory, wherein in responding to a read request requiring multiple data burst over the memory bus, data from each of said multiple data bursts is stored in a respective memory of said cache memory.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modified Bronson by the teaching of Schulz, because to include for the memory controller system, method and programmable logical device, comprising:

the cache memory, wherein in responding to the read request requiring multiple data burst over the memory bus, data from each of said multiple data bursts is stored in the respective memory of said cache memory, would enable the implementation of pre-fetching and improve the performance of the computer system.

As per claims 2 and 8, Bronson as modified teaches the memory controller system, method and programmable logical device, comprising wherein, when returning data to the respective device from which the read request requiring multiple data bursts over the memory bus was received and interleave the reading of said multiple data burst from a plurality of buffer banks (Schulz, column 3, lines 41-55 and column 8, line 48 to column 9, line 48. where "interleave the reading of said multiple data burst from a plurality of buffer banks" is read on "data is read out from a first part of one of said buffers, then data is read out from at least one other of said buffers, then data is read out from a second part of said one of said buffers"), wherein interleaving the reading of data increase bandwidth performance of the overall memory subsystems.

As per claims 3 and 9, Bronson as modified teaches the memory controller system, method and programmable logical device, comprising wherein said cache memory is coupled to said memory interface and storing data from each of said multiple data bursts in the respective memory in said cache memory (Schulz, Figure 2, column 1, line 56 to column 2, line 10 and column 5, lines 37-62).

As per claims 4 and 10, Bronson as modified teaches the memory controller system, method and programmable logical device, comprising wherein for the I/O bus unit comprise of two sets of data buffers and one of said buffer set is for PIO/MMIO read reply data (Bronson, column 4, line 40 to column 5, line 22, where "two sets of buffers" is read on "respective plurality of buffers" and "PIO/MMIO read reply data" is read on

"data from each of said multiple data bursts" and Schulz, column 1, line 56 to column 2, line 10).

As per claims 6 and 12, Bronson as modified teaches the memory controller system, method and programmable logical device, comprising wherein the memory manager is a SDRAM memory manager, and said memory manager is suitable for connection to a SDRAM memory device over said memory bus (Bronson, Figure 1 and column 5, lines 45-52).

4. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson et al. (US Patent 6,279,064) in view of Schulz (US Patent 6,959,374), as applied to claims 1-4, 6-10 and 12-13, further in view of Secatch et al. (US Pub.: 2003/0131162).

As per claims 5 and 11, Bronson as modified teaches the memory controller system, method and programmable logical device, comprising:

a cache memory for buffering (Schulz, Figure 2);

receiving the read request requiring multiple memory burst over the memory bus (Schulz, column 1, line 65 to column 2, line 10); and

the control unit allocates each of said memory bursts to a respective one of said buffers (Schulz, column 4, line 48 to column 5, line 10).

Bronson as modified does not teach the memory controller system, method and programmable logical device, comprising the control logic determining whether a received read access request is a wrapping request.

Secatch teaches a buffering system and method comprising:

a non-destructive FIFO buffer to be used as a cache; and

receiving a loop of instruction, wherein the loop instruction comprise of a "for" code, to be executed a desired number of times ([0002]-[0008] on page 1, where "loop of instructions" is read on "wrapping request").

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Bronson as modified to include the memory controller system, method and programmable logical device, comprising:

the non-destructive FIFO buffer to be used as the cache and the control unit receiving and determining whether a received read access request is a loop instruction, comprising of a "for" code, which requires multiple memory bursts.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modified Bronson as modified by the teaching of Secatch, because including the memory controller system, method and programmable logical device, comprising:

the non-destructive FIFO buffer to be used as the cache and the control unit receiving and determining whether a received read access request is a loop instruction, comprising of a "for" code, which requires multiple memory bursts, would improve the throughput and reduce processing overhead by simply resetting the read pointer to the

address of the FIFO containing the first instruction of the loop after the read pointer has been incremented to the address containing the last instruction in of the loop.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671 and email is chunkuan.lee@uspto.gov. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Popovici Dov can be reached on (571)272-4083. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Mailed responses to this action should be sent to:

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Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

(571) 273-8300

Hand-delivered responses should be brought to:

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C.K.L.
11/29/2005

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